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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,217	07/24/2003	Christophe F. Pomarede	ASMEX.284DV1	9650

20995 7590 06/30/2004

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
NOVACEK, CHRISTY L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,217	POMAREDE ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this c mmunication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the communication filed July 24, 2003.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 9, 10 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Moore (US 6,649,543).

Regarding claim 1, Moore discloses forming a gate dielectric (18) over a semiconductor substrate (16), exposing the gate dielectric to a source of nitrogen excited species, wherein exposing incorporates less than about 10% atomic nitrogen at a depth of greater than about 10 Δ from an upper surface of the gate dielectric and depositing a silicon-containing gate electrode (26/28) over the gate dielectric after exposing the gate dielectric to the source of nitrogen excited species (Fig. 4-7; col. 3, ln. 3 – col. 6, ln. 21).

Regarding claim 9, Moore discloses forming an oxide layer (18) over a semiconductor substrate (16), exposing an upper surface of the oxide layer to products of a plasma such that less than 10 atomic % of the products of the plasma are incorporated into the oxide layer at a depth of greater than 10 Δ from the upper surface and depositing a silicon-containing gate electrode

(26/28) over the upper surface after exposing the upper surface to the products of the plasma (Fig. 4-7; col. 3, ln. 3 – col. 6, ln. 21).

Regarding claim 10, Moore discloses that the oxide layer serves as a gate dielectric.

Regarding claim 15, Moore discloses that the products of the plasma include nitrogen excited species (col. 4, ln. 8-20).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore (US 6,649,543) in view of Ma et al. (US 6,297,539).

Regarding claims 2, 3 and 11, Moore discloses that the gate dielectric comprises silicon oxide and does not disclose that the gate dielectric includes a metal oxide. Like Moore, Ma discloses a method of making a gate oxide for a MOS transistor. Ma teaches that it is advantageous to form the gate oxide from a metal oxide, such as zirconium oxide, instead of forming it of silicon oxide because the metal oxide offers the benefit of allowing the gate oxide to be thicker, which reduces the problem of high tunneling current through the gate oxide (col. 1, ln. 16-53). At the time of the invention, it would have been obvious to one of ordinary skill in the art to substitute the silicon gate oxide of Moore with a metal gate oxide such as zirconium

oxide because Ma teaches that a metal gate oxide offers the advantage of lessening the possibility of having high tunneling current go through the gate oxide.

Claims 4-6 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore (US 6,649,543) in view of Ma et al. (US 6,297,539) and Setton (US 6,727,148).

Regarding claims 4 and 12, Moore does not disclose exposing the surface of the substrate to a source of nitrogen excited species prior to forming the gate dielectric. For the reasons cited above in reference to claims 2, 3 and 11, at the time of the invention, it would have been obvious to one of ordinary skill in the art to substitute the silicon oxide gate layer of Moore with a metal oxide layer, as is taught by Ma. Like Moore and Ma, Setton discloses a method of making a gate oxide for a MOS transistor. Setton teaches that when forming a metal oxide gate dielectric layer on a semiconductor substrate, there is a likelihood that the surface of the substrate will be oxidized, thus causing a problem of increasing high tunneling current through the dielectric. In order to avoid this problem, Setton exposes the surface of the substrate to a source of nitrogen excited species (plasma) prior to forming the gate dielectric to create an interfacial layer of silicon nitride on the substrate (col. 1, ln. 21-57; col. 3, ln. 6-27). The interfacial layer prevents high tunneling current. At the time of the invention, it would have been obvious to one of ordinary skill in the art to expose the substrate surface to nitrogen excited species prior to forming the gate dielectric of Moore because Setton teaches that by forming an interfacial layer between the substrate and the gate dielectric, high tunneling current through the gate dielectric can be prevented.

Regarding claims 5 and 13, Setton discloses that exposing the surface of the substrate to nitrogen excited species can form a silicon nitride layer on the surface of the substrate (thus, no silicon oxynitride is formed) (col. 3, ln. 6-27).

Regarding claims 6 and 14, Ma discloses that the metal oxide layer can be deposited by atomic layer deposition (col. 3, ln. 11-34).

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore (US 6,649,543) in view of Aoki et al. (US 6,744,104).

Regarding claim 7, Moore does not disclose that the silicon-containing gate electrode includes silicon-germanium. Like Moore, Aoki discloses a method of forming a MOS transistor. Aoki teaches that by forming a portion of the gate electrode of silicon-germanium by CVD, the transistor can be protected against leakage of a doped impurity into the channel region (col. 3, ln. 15-22). At the time of the invention, it would have been obvious to one of ordinary skill in the art to substitute the silicon-containing gate electrode of Moore with a silicon-germanium gate, because Aoki teaches that a silicon-germanium gate offers the advantage of protecting the transistor against leakage of a doped impurity into the channel region.

Regarding claim 8, Aoki discloses that the silicon-germanium gate is formed by flowing germane (GeH_4) over the gate dielectric (col. 14, ln. 15-20).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
June 26, 2004

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800